Star Sensor Design: Interface Circuit and VHDL Implementation on FPGA

Neha K
PES Institute of Technology, Bangalore
nehakanchetti96@gmail.com

Nikhil P V S
PES Institute of Technology, Bangalore
nikhilpodila.94@gmail.com

Mayuresh S
Indian Institute of Astrophysics, Bangalore
mayuresh@iiap.res.in

Dr. V. K. Agrawal
PES Institute of Technology, Bangalore
vk.agrawal@pes.edu

Dr. Jayant Murthy
Indian Institute of Astrophysics, Bangalore
murthy@iiap.res.in

Abstract – A Star Sensor is a main component of attitude determination subsystem in small satellites. This paper implements an interface technology for a Complimentary Metal-Oxide Semiconductor (CMOS) Image Sensor with 1024 by 1024 pixels, for utilization as a Star Sensor. Firstly, an interface PCB is designed for compatibility between Logic unit and the CMOS sensor. A VHDL implementation is performed to communicate with the CMOS sensor and retrieve the required image frames at a rate of 9.5 (Hz). This technology is portable to various hardware, and is flexible to most CMOS Image Sensors and High-speed Processor Systems.

Index Terms – Star sensor, timing sequence, sensor interface, VHDL

INTRODUCTION

Star Sensor determines the attitude of a Satellite revolving around the earth. This data is used by an actuator to reorient the satellite to its desired attitude. Star Sensor consists of an Image Sensor which captures star images that are compared with a star catalog. Star Identification and Quaternion Estimation Algorithms are then used to find the position of stars with respect to a reference frame. This paper implements the sequence of pulses to be applied on the control pins of an Image Sensor to acquire data for processing. The Sensor used is STAR 1000 1M Pixel Radiation Hardened CMOS Image Sensor with On Chip Fixed Pattern Noise Correction and 10 bit ADC [1]. The FPGA used for interfacing is the Xilinx Virtex-5 XCV5FX110T and Spartan-6 XQ6SLX150T, and the latter will be used for complete implementation of the Star Sensor.

Image Acquisition comprises of Reset and Readout processes. STAR 1000 has 1024×1024 Active Pixels with Row wise Reset and Pixel wise Readout. Image frames are captured at the rate of 9.5(Hz) continuously upon the request command of an On-board Computer.

Reset process: Applying a reset signal to each row in order to clear the frame for the next readout. Each row has an Exposure time of 104.8576(ms) to capture the image. This process is done in a sequential manner such that at the end of reset of last row, the first row is set for readout. Readout process includes:

Line Readout: Applying S, R, Ld_Y (Latch) and Reset signals, causes a pixel row (of Y address) to be stored in the Column Gain Amplifier. This Column Amplifiercompares the signals with the reset signal to correct distortion. This process also inherently resets the row.

Difference between the voltage levels of the signals is sent to an Output Amplifier.

Pixel Readout: Each pixel signal of the above selected row is sent through the Program Gain Amplifier, consecutively, at a rate of 90(ns) per pixel.

Analog to Digital conversion takes place and the pixel signal is converted to 10 bit data which appears at D0-D9 pins.

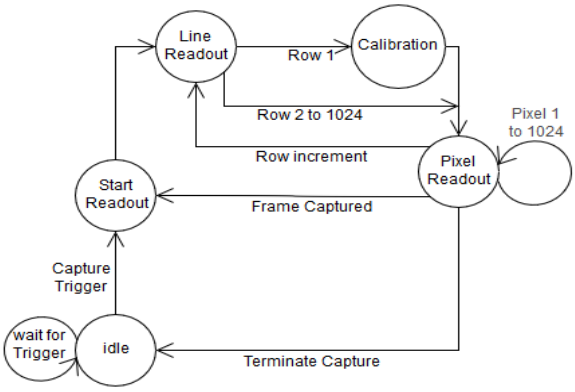

FIGURE 1.STATE MACHINE OF IMAGE ACQUISITION

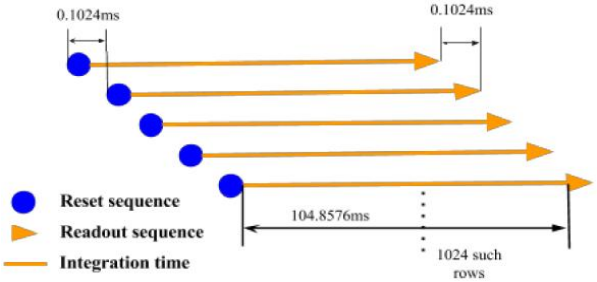

FIGURE 2.TIMING SEQUENCE OF RESET AND READOUT

STAR SENSOR INTERFACE PCB

The Star Sensor PCB Board is a double layer PCB with SMD components. The PCB contains:
Chip Socket for the Star 1000 sensor. STAR 1000 Sensor has an offset of 200(µm) below and 52(µm) to the left of Centre of Cavity from the Center of Silicium. Chip Socket is shifted by 200(µm) above the Center of Cavity of the PCB to compensate for the offset, which ensures a higher accuracy of image captured. Voltage Regulator of 3.3(V) creates compatibility between the STAR 1000 Sensor and the FPGA Development Boards.SMT 40 pin Connector is used for the interfacing of control pins including the address and data pins of the pixels to the FPGA Boards.

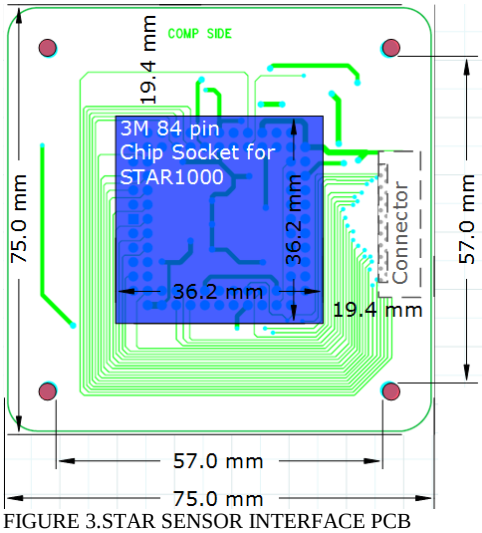

FIGURE 3.STAR SENSOR INTERFACE PCB

VHDL IMPLEMENTATION OF RESET AND READOUT SEQUENCE

As Microprocessors and Microcontrollers execute operations sequentially, the reset and readout signals have non-simultaneous execution. As these signals are in the order of nanoseconds, it is preferable to use parallel logic system like FPGA over Microprocessors.The FPGAs are programmed using VHDL and the tests were performed on the board and the Xilinx ISim [2].
The VHDL is implemented asynchronously, with a Master Clock (clk) having a Time Period of 5 (ns). Implementation of all the signals has been done with respect to clk. A maximum signal time margin of 50% has been considered, that is, each signal has a delay of 50% greater than the optimal delay time to account for clock and communication errors. The VHDL code implemented consists of a counter register, which is initialized to 0 for every pixel row, and stores the number of rising edges of clk triggered since the initialization. All signals, delays and events in the Reset and Readout sequence begin and end only when the counter register has been updated at every rising edge of clk.

The implementation consists of 10 ports. The input ports are:

- clk_in: Clock signal from the Digital Clock Module and a Quartz crystal.
- mpTrig: Trigger from the Satellite On-Board Computer to start Attitude Determination process.
- The output ports are:
- addr: Address bus to sensor.
- Ld_Y, Ld_X: Address Latch signals to sensor.
- S, R, Reset, Cal: Various reset and readout sequence signals to sensor.
- Clk_X: Clock for Pixel readout to sensor. Based on clk.
- mpBusy: Busy status control signal to Satellite On-Board Computer

The VHDL code was tested using the Xilinx ISim tool, and the results were obtained as expected. The code was also executed on a custom development board using Spartan 6 FPGA and the output signals were tested using a Digital Oscilloscope.
This implementation has an advantage of being easily portable to other CMOS Image Sensors. Porting can be done by changing the Master clock and the counter register trigger values for the reset and readout signals, as required.

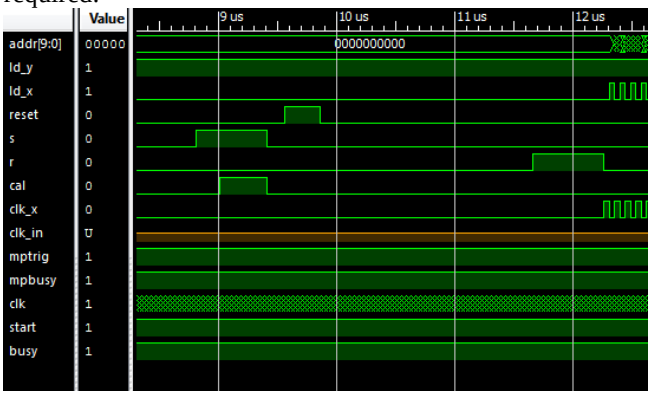

FIGURE 4.TIMING DIAGRAM SIMULATION

ACKNOWLEDGEMENTS

We would like to thank Indian Institute of Astrophysics and PES Institute of Technology for their support in this research project. We would also like to thank Prof. K N B Murthy, PES University for encouragement.

REFERENCES

[1] ON Semiconductor Star 1000 Datasheet [Online]. Available: HTTP://WWW.ONSEMI.COM/PUB_LINK/COLLATERAL/NOIS1SM1000A-D.PDF
[2] V. Sklyarov et al. “Synthesis and Optimization of FPGA-Based Systems”